REMARKS

Claims 41 and 43-52 are pending in the above-referenced application. All stand rejected. Claims 41, 45, 50 and 52 are amended. Such amendments do not add any new matter.

Applicant notes that the Examiner states that pages 278-280 from *Wolf,* volume 1 were not provided with Applicant's last paper. While Applicant believes such pages were included, such pages are again provided and the argument from that paper relating to such pages is respectfully reasserted in this action.

Rejection under 35 U.S.C. §102

Kurimoto

Claims 41, 45, 46, 50 stand rejected under 35 U.S.C. §102(b) as being anticipated by Kurimoto (5,306,655). Applicant traverses.

Claim 41 recites, in pertinent part, "forming sidewall spacers comprising nitride on the gate electrode's sidewalls" and "after forming the sidewall spacers comprising nitride and prior to forming source/drain regions, exposing the substrate to oxidizing conditions."

Claim 45 recites, among other things, "forming sidewall spacers laterally adjacent the conductive gate structure's sidewalls sufficiently to cover all conductive material comprising the sidewalls" and "after forming the oxidation resistant sidewall spacers and prior to forming source/drain regions adjacent the gate structure, conducting an oxidizing step." Claim 46 depends from Claim 45.

Claim 50 recites, among other things, "anisotropically etching the non-oxide material to form spacers on the sidewalls" and "prior to forming source/drain regions, exposing the substrate to oxidizing conditions."

In contrast, Kurimoto teaches that "the side faces of gate electrode 5f are oxidized" (col. 13, lines 42-43) prior to covering the gate electrode with insulating film 10. Such structure is depicted in Fig. 13(c). In addition, Kurimoto teaches that in step (e) "ion implantation is executed to ... form n-type highly doped diffusion regions 3" and that in subsequent step (f) "oxidation is executed of the lower parts of the right and left side faces of gate electrode 5f" (col. 13, lines 53-56 and 59-61, respectively).

Thus it is seen that Kurimoto fails to teach or even suggest at least two aspects of the instant invention recited in each of Claims 41, 45 and 50. Kurimoto (1) fails to teach forming a silicon nitride or any other oxidation resistant spacer **on** the sidewalls of the gate electrode, and (2) fails to provide oxidizing conditions **prior to** forming highly doped diffusion regions that one of ordinary skill in the art would recognize as source/drain regions (see, Fig. 13d, 13e, and 13f).

M.P.E.P. §706.02 states that "for anticipation under U.S.C. §102, the reference must teach every aspect of the claimed invention either explicitly or impliedly." Since it is shown above that Kurimoto fails to meet this standard, with regard to Claims 41, 45 and 50, the rejection of such claims under §102 must be withdrawn. Claim 46 depends from Claim 45, therefore for at least the same reasons as for Claim 45, the

rejection of Claim 46 must be withdrawn. Action to this effect is requested.

Verhaar with Hiroki et al

Claims 41, 45, 46, 50 stand rejected under 35 U.S.C. §102(b) as being anticipated by Verhaar (5,015,598), with Hiroki et al (5,512,771, hereinafter "Hiroki") as an evidence, or alternatively under 35 U.S.C. §103(a). Applicant traverses.

Regarding the §102 rejection, Verhaar, like Kurimoto, teaches providing oxidizing conditions after forming source/drain regions proximate the gate electrode. Specifically Fig. 4 depicts ion implantation 21 forming source/drain regions 23, see column 5, lines 19-24, and Fig. 5 depicts the structure of Fig. 4 after a thermal oxidation to form silicon oxide layer 24, ibid. lines 39-46.

As presented above, each of Claims 41, 45 and 50 explicitly recite, that such oxidizing conditions are provided prior to forming source/drain regions. Claim 46, depending from Claim 45, includes such a recital through this dependence.

Thus for at least the failure to teach or suggest providing the oxidizing conditions prior to forming the source drain regions, it is evident that Verhaar does not meet that standard for a rejection under §102 as provided in M.P.E.P. §706.02 and the instant rejection of Claims 41, 45, 46 and 50 must be withdrawn.

Regarding §103 rejection, as stated above, Verhaar fails to teach or even suggest all aspects of the invention as recited in Claims 41, 45, 46

and 50. Specifically Verhaar fails to teach or suggest providing oxidizing conditions before or prior to forming source/drain regions. With regard to Hiroki, Figs. 6A and 6B, as well as the text at col. 12, lines 10-21 indicate that Hiroki teaches forming an oxide film 6 adjacent or on the gate electrode sidewalls, rather than the silicon nitride or oxidation resistant film recited in Applicant's claims. The Examiner, however, alleges that it would be obvious to one of ordinary skill in the art to combine the oxidation of Hiroki with the structure of Verhaar to form a smiling gate. Applicant disagrees

Applicant notes that Hiroki provides the oxidizing conditions prior to forming source/drain regions. Applicant respectfully directs the Examiner to Verhaar at column 5, lines 31-36, where Verhaar essentially states that performing the oxidation after forming the source/drain regions is necessary "to ensure a satisfactory operation of the device." Thus such a modification of Verhaar would render it unsatisfactory for its intended purpose, which, according to M.P.E.P. §2143.01 necessarily makes such a combination NON-OBVIOUS. It necessarily follows then that the combination of Verhaar and Hiroki does not meet the standard for a rejection under §103 and hence the rejection of Claims 41, 45, 46 and 50 must be withdrawn.

Rejections under 35 U.S.C. §103:

Kurimoto or Verhaar/Hiroki in view of Pintchovski et al

Claims 43, 47 stand rejected under U.S.C. §103(a) as being unpatentable over either Kurimoto or Verhaar/Hiroki, in view of Pintchovski et al (5,126,283, hereinafter "Pintchovski").

Claims 43 and 47 depend from Claims 41 and 45 respectively. As shown above, Kurimoto fails to teach or even suggest at least two aspects of the invention recited in Claims 41 and 45. The Examiner does not suggest that Pintchovski provides a remedy for these deficiencies of Kurimoto, nor does Pintchovski in fact provide such remedies. Therefore the combination of Kurimoto and Pintchovski CANNOT make the invention of Claims 43 or 47 obvious, failing to meet the standard for such a rejection.

The Examiner suggests as an alternative rejection the combination of Verhaar/Hiroki, in view of Pintchovski. However, as shown above, the combination of Verhaar with Hiroki is improper as it would render Verhaar unsatisfactory for its intended purpose. Again the Examiner does not suggest, nor does Pintchovski in fact provide such a remedy for the deficiency of Verhaar/Hiroki. Therefore the combination of Verhaar/Hiroki with Pintchovski remains flawed and cannot meet the standard for a rejection under §103. Thus Applicant requests that the rejection of Claims 53 and 47 be withdrawn.

Kurimoto or Verhaar/Hiroki in view of Pintchovski and further of Brigham et al and Kumagai et al

Claims 44, 48, 49, 51, 52 stand rejected under U.S.C. §103(a) as being unpatentable over either Kurimoto or Verhaar/Hiroki, in view of Pintchovski, as applied to claims 41, 43, 45-57, 50, above, and further of Brigham et al. (5,714,413, hereinafter "Brigham") and Kumagai et al (5,430,313, hereinafter "Brigham"). Applicant traverses.

Claims 44, 48, 49 and 51 depend from Claims 41, 45 and 50, respectively. Each then includes, at least, the aspects of such independent claims discussed above. Claim 52 is an independent claim that recites the previously discussed aspects of Claims 41, 45 and 50, in alternative language. Thus Claim 52 recites "a first barrier material contacting the sidewalls [of the gate electrode]" and prior to forming source/drain regions proximate the gate structure, exposing the substrate to oxidation conditions." These recited aspects of Claim 52, like the aspects of Claims 41, 45 and 50, discussed above, are not taught or suggested by any of Kurimoto, Verhaar/Hiroki or Pintchovski taken alone or in any combination. The Examiner does not suggest, nor do Brigham or Kumagai in fact, remedy the several deficiencies the Applicant has shown for Kurimoto, Verhaar/Hiroki or Pintchovski. Therefore, any combination of Brigham or Kumagai with any or all of Kurimoto, Verhaar/Hiroki or Pintchovski will necessarily be deficient and incapable of meeting the standard for a rejection under §103. It follows then that the rejection of Claims 44, 48, 49, 51 and 52 must be withdrawn.

Objected to Claims

Claim 41, line 2, stands objected to for having typographical error, since the term "gate" should be –gate electrode—so that it is consistent with later recitation as in line 3 of claim 41. Applicant disagrees.

First, the term referred to by the Examiner should be correctly stated as "transistor gate." Second, it is well known in the semiconductor arts, that the term "transistor gate" encompasses a number of components. For example, in the context of Claim 41, a skilled artisan would understand the term "transistor gate" at line 2 to include the terms "gate electrode" and "gate dielectric" at line 3 of such claim. Thus Applicant respectfully asserts that Claim 41 is absent a typographical error and is correct as currently presented.

In summary, Applicant having responded to each of the rejections and objections, respectfully asserts that Claims 41 and 43.52 are in condition for allowance. Action to that effect is earnestly sought. If, however the Examiner's next action is anything other than a Notice of Allowance, the Examiner is requested to call the undersigned to schedule a telephonic interview. The undersigned is available during normal business hours, Pacific Coast Time.

Respectfully submitted,

Dated: Sep 14, 2001

By: Bernard Berman

Bernard Berman
Reg. No. 37,279

EL844050489

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/059,644
Filing Date ..... April 13, 1998
Inventor ..... Pai-Hung Pan
Assignee ..... Micron Technology, Inc.
Group Art Unit 2822
Examiner ..... M. Trinh
Attorney's Docket No. MI22-898
Title: Semiconductor Processing Methods of Forming a Conductive Gate and Line

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO JUNE 20, 2001 OFFICE ACTION

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

41. (Amended) A semiconductor processing method of forming a conductive transistor gate over a substrate comprising:

forming a conductive gate electrode over a gate dielectric layer on a substrate, the gate electrode having sidewalls and an interface with the gate dielectric layer;

forming sidewall spacers comprising nitride ~~over~~ on the gate electrode's sidewalls, the sidewall spacers joining with the gate dielectric layer; and

after forming the sidewall spacers comprising nitride and prior to forming source/drain regions, exposing the substrate to oxidizing conditions effective to channel oxidants through the gate dielectric layer and underneath the sidewall spacers joined therewith, wherein a potion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric layer, is oxidized.

45. (Amended) A semiconductor processing method of forming a conductive gate comprising:

forming a conductive gate structure on a first layer which is disposed on a substrate, the gate structure comprising a gate electrode having sidewalls and an interface with the first layer;

forming sidewall spacers ~~latterly~~ laterally adjacent the conductive gate structure's sidewalls sufficiently to cover all conductive material comprising the sidewalls, the sidewall spacers comprising an oxidation resistant material; and

after forming the oxidation resistant sidewall spacers and prior to forming source/drain regions adjacent the gate structure, conducting an oxidizing step by channeling oxidants through the first layer which is outwardly exposed laterally proximate the oxidation resistant sidewall spacers wherein the oxidation resistant sidewall spacers provide that only a portion of the gate electrode, adjacent the oxidation resistant sidewall spacers and at the interface with the first layer is oxidized.

50. (Amended) A semiconductor processing method of forming a conductive transistor gate over a substrate comprising:

forming a dielectric layer on a substrate;

forming a conductive gate structure over the dielectric layer, the gate structure having sidewalls defining a lateral dimension of the gate structure;

forming non-oxide material over the gate structure and the dielectric layer;

anisotropically etching the non-oxide material to form spacers ~~over~~ on the sidewalls, the spacers laterally adjacent the gate structure and joining with the gate dielectric layer there at; and

~~after forming the spacers~~ prior to forming source/drain regions, exposing the substrate to oxidizing conditions effective to oxidize only that portion of the gate structure adjacent the spacers and the dielectric layer.

52. (Amended) A semiconductor processing method of forming a conductive gate comprising:

forming a gate structure atop a substrate having a dielectric layer thereon, at least a portion of the gate structure being conductive, the conductive portion comprising:

a polysilicon layer,

an overlying metal, and

a reaction barrier layer interposed between the polysilicon and the overlying metal;

covering a top and sidewalls of the gate structure with an oxidation resistant material, said covering comprising:

a first barrier material contacting the sidewalls, and

a second barrier material disposed over the first barrier material,

anisotropically etching the oxidation resistant material to a degree sufficient to leave the oxidation resistant material laterally adjacent to and covering all of the sidewalls of the gate structure while exposing the dielectric layer adjacent the gate structure; and

prior to forming source/drain regions proximate the gate structure, exposing the substrate to oxidation conditions effective to oxidize a portion of the gate structure laterally adjacent the covered sidewalls and adjacent the dielectric layer.